REMARKS

Claim Rejections

Claims 25-28, 33-34, and 36-37 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. (U.S. 6,765,152) in view of Ahn et al. (U.S. 6,765,152). Claims 29-30 and 35 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. and Ahn et al. in view of Klein et al. (U.S. 2004/0145051). Claim 31 is rejected under 35 U.S.C. §103(a) as being unpatentable over Giri et al. and Ahn et al. in view of Kikuma et al. (U.S. 6,621,169). Claim 32 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. and Ahn et al. in view of Koopmans (U.S. 2004/0035840). Claims 38 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. and Ahn et al. in view of Higgins III (U.S. 5,583,377).

Claim Amendments

By this Amendment, Applicant has amended claim 25 of this application and added claim 39. It is believed that the amended and new claims specifically set forth each element of Applicant's invention in full compliance with 35 U.S.C. § 112 (*See, e.g.,* p. 6, ll. 9-12), and define subject matter that is patentably distinguishable over the cited prior art, taken individually or in combination.

In the present invention, the dummy die 130 is a silicon substrate having no electrically calculating function. As shown in Fig. 4, the dummy die has a redistribution layer 133 formed thereon providing a tough structure for mounting a flip chip 120 and connecting bonding wires 137, also providing zero stress between the flip chip 120 and the dummy die 130. The dummy die also includes a bottom surface having a high thermal-conducting metal layer 233 configured to dissipate heat from the chip package. Advantageously, the metal layer further reduces the stress between the flip chip and the dummy die. In one preferred embodiment, the high thermal-conducting metal layer is formed by sputtering to enhance heat dissipation.

The primary reference to Giri et al. discloses a multi-chip module having chips on two sides including a frame (12), a large semiconductor device (22) located above the thin-film structure, a thin-film structure (18), and a plurality of semiconductor devices (20) located below the thin-film structure. The thin-film

structure (18) is a soft multilayer polyimide on which the large semiconductor device (22) and the plurality of semiconductor devices (20) are mounted. As admitted by the Examiner, the thin-film structure of Giri et al. is not a dummy die which is a silicon substrate having no electrically calculating function. Giri et al. further teaches that "chip 20, 22 connect to contact pads 26, 24 by small solder balls." These contact pads and small solder pads should not be confused with a high thermal-conducting metal layer.

Giri et al. do not teach or suggest a dummy die further including a high thermal-conducting metal layer on the bottom of an exposed surface of the dummy die. Giri et al. also do not teach a spluttered metal layer.

The secondary reference to Ahn et al. teaches a silicon interposer substrate (100) used to carry both memory chips (110) and a microprocessor (120).

Ahn et al. do not teach or suggest a dummy die including a high thermal-conducting metal layer on the bottom of an exposed surface of the dummy die. Ahn et al. also do not teach or suggest a spluttered metal layer on the bottom surface of a dummy die.

The secondary reference to Klein et al. discloses a semiconductor component having stacked dice and including a base die (12) a first secondary die (14-1) a second secondary die (14-2), terminal contacts (18) and a package substrate (120). There is no indication that either of the first secondary or the second secondary die is a chip.

Klein et al. does not teach a dummy die including a high thermal-conducting metal layer on the bottom of an exposed surface of a dummy die. Klein et al. also do not teach or suggest a spluttered metal layer on the bottom surface of a dummy die.

The secondary reference to Kikuma et al. discloses a stacked semiconductor device including a substrate (108), a semiconductor chip (102) located on the substrate and having a redistribution layer (114), a chip (104) located above the redistribution layer, bonding wires (116) connecting the distribution layer to the substrate, and an adhesive (112) connecting the semiconductor chip to the substrate.

Kikuma et al. do not teach or suggest a silicon substrate having no electrically calculating function, the dummy die further including a high

thermal-conducting metal layer on the bottom of an exposed surface of the dummy die. Kikuma et al. also do not teach or suggest a spluttered metal layer on the bottom surface of a dummy die.

The secondary reference to Koopmans discloses a component installation removal and replacement apparatus including a substrate (34), connected to contacts (26, 28) by a redistribution layer (21), the redistribution layer is located on a flip-chip (10) and includes first and second dielectric layers (22, 24).

Koopmans does not teach or suggest a dummy die including a high thermal-conducting metal layer on the bottom of an exposed surface of the dummy die. Koopmans also does not teach or suggest a spluttered metal layer on the bottom surface of a dummy die.

The secondary reference to Higgins, III teaches a pad array semiconductor device including a substrate (42) with an opening (20) having a ledge (44), a heat sink (46) located in an opening, and a semiconductor die (13) located on the heat sink.

Higgins, III does not teach or suggest a silicon substrate having no electrically calculating function, the dummy die further including a high thermal-conducting metal layer on the bottom of an exposed surface of the dummy die. Higgins, III also does not teach or suggest a spluttered metal layer on the bottom surface of a dummy die.

Even if the teachings of Giri et al., Ahn et al., Klein et al., Kikuma et al., Koopmans, and Higgins, III were combined, as suggested by the Examiner, the resultant combination does not suggest: a dummy die being a silicon substrate having no electrically calculating function and having a redistribution layer, the dummy die further including a high thermal-conducting metal layer on the bottom of an exposed surface of the dummy die; nor does the combination suggest a spluttered metal layer on the bottom surface of a dummy die.

It is a basic principle of U.S. patent law that it is improper to arbitrarily pick and choose prior art patents and combine selected portions of the selected patents on the basis of Applicant's disclosure to create a hypothetical combination which allegedly renders a claim obvious, unless there is some direction in the selected prior art patents to combine the selected teachings in a manner so as to negate the patentability of the claimed subject matter. This principle was enunciated over

40 years ago by the Court of Customs and Patent Appeals in In re Rothermel and Waddell, 125 USPQ 328 (CCPA 1960) wherein the court stated, at page 331:

> The examiner and the board in rejecting the appealed claims did so by what appears to us to be a piecemeal reconstruction of the prior art patents in the light of appellants' disclosure. ... It is easy now to attribute to this prior art the knowledge which was first made available by appellants and then to assume that it would have been obvious to one having the ordinary skill in the art to make these suggested reconstructions. While such a reconstruction of the art may be an alluring way to rationalize a rejection of the claims, it is not the type of rejection which the statute authorizes.

The same conclusion was later reached by the Court of Appeals for the Federal Circuit in Orthopedic Equipment Company Inc. v. United States, 217 USPQ 193 (Fed.Cir. 1983). In that decision, the court stated, at page 199:

> As has been previously explained, the available art shows each of the elements of the claims in suit. Armed with this information, would it then be non-obvious to this person of ordinary skill in the art to coordinate these elements in the same manner as the claims in suit? The difficulty which attaches to all honest attempts to answer this question can be attributed to the strong temptation to rely on hindsight while undertaking this evaluation. It is wrong to use the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit. Monday morning quarterbacking is quite improper when resolving the question of non-obviousness in a court of law.

In In re Geiger, 2 USPQ2d, 1276 (Fed.Cir. 1987) the court stated, at page 1278:

> We agree with appellant that the PTO has failed to establish a *prima facie* case of obviousness. Obviousness cannot be established by combining the teachings of the prior art to produce the claimed

invention, absent some teaching suggestion or incentive supporting the combination.

Applicant submits that there is not the slightest suggestion in either Giri et al., Ahn et al., Klein et al., Kikuma et al., Koopmans, or Higgins, III that their respective teachings may be combined as suggested by the Examiner. Case law is clear that, absent any such teaching or suggestion in the prior art, such a combination cannot be made under 35 U.S.C. § 103.

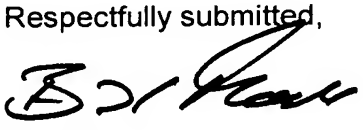
Neither Giri et al., Ahn et al., Klein et al., Kikuma et al., Koopmans, nor Higgins, III disclose, or suggest a modification of their specifically disclosed structures that would lead one having ordinary skill in the art to arrive at Applicant's claimed structure. Applicant hereby respectfully submits that no combination of the cited prior art renders obvious Applicant's amended claims.

Summary

In view of the foregoing amendments and remarks, Applicant submits that this application is now in condition for allowance and such action is respectfully requested. Should any points remain in issue, which the Examiner feels could best be resolved by either a personal or a telephone interview, it is urged that Applicant's local attorney be contacted at the exchange listed below.

Respectfully submitted,

Date: February 15, 2006

By: 

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